AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 2-3, 11-14 and 17-18 as follows:

LISTING OF CLAIMS:

1. (Original) A semiconductor integrated circuit comprising:

a first logic section and a second logic section;

a functional block connected between said first logic section and said second logic section;

a scan path that includes, between an output of said first logic section and an input of said functional block, a parallel path and a serial shift path for serially transferring data, and that includes a plurality of first selectors for switching and connecting one of the output of said first logic section and said serial shift path to the input of said functional block, and a plurality of flip-flops for storing the data; and

a plurality of second selectors connected into said serial shift path of said scan path, for switching and connecting one of an output of said functional block and said serial shift path to an input of said second logic section, wherein

test data is provided from said serial shift path of said scan path to said functional block via said second selectors, and data output from said functional block is output via said second selectors after switching said second selectors.

2. (Currently Amended) The semiconductor integrated circuit according to claim 1, wherein said flip-flops on said serial shift path are connected to the

outside of the parallel path between the output of said first logic section and the input of said functional block.

3. (Currently Amended) The semiconductor integrated circuit according to claim 1, wherein said functional block consists of a RAM (Random Access Memory), and said scan path includes a plurality of inverters interposed into said serial shift path to change the data to be provided to said RAM by alternating to all ~~zero~~ zeroes or all ~~one-by-one time~~ ones each shift operation clock cycle.

4. (Original) The semiconductor integrated circuit according to claim 3, wherein said inverters are connected to the output of said second selectors.

5. (Original) The semiconductor integrated circuit according to claim 3, wherein said scan path further comprises a third selector for feeding an output of said serial shift path back to an input of said serial shift path.

6. (Original) The semiconductor integrated circuit according to claim 5, further comprising a gate circuit for detecting that the data output from said functional block via said second selectors take a specified value.

7. (Original) The semiconductor integrated circuit according to claim 5, further comprising a gate circuit for detecting that the data output from said functional block via said inverters take a specified value.

8. (Original) The semiconductor integrated circuit according to claim 5, further comprising a gate circuit for detecting that the data output from said functional block via said first selectors take a specified value.

9. (Original) The semiconductor integrated circuit according to claim 5, further comprising a gate circuit for detecting that the data output from said functional block and stored in said flip-flops take a specified value.

10. (Original) The semiconductor integrated circuit according to claim 1, wherein said flip-flops on said serial shift path of said scan path have inputs of said flip-flops connected to outputs of the second selectors, and have outputs of said flip-flops connected to the input of said second logic section.

11. (Currently Amended) The semiconductor integrated circuit according to claim 10, wherein said functional block consists of a RAM, and said semiconductor integrated circuit further comprises:

a plurality of inverters interposed into said serial shift path of said scan path to change the data to be provided to said RAM by alternating to all ~~zero~~ zeroes or all ~~one-by-one-time~~ ones each shift operation clock cycle;

a third selector for feeding an output of said serial shift path of said scan path back to an input of said serial shift path; and

a gate circuit for detecting that data output from said RAM via said second selectors take a specified value.

12. (Currently Amended) The semiconductor integrated circuit according to claim 10, wherein said functional block consists of a RAM, and said semiconductor integrated circuit further comprises:

a plurality of inverters interposed into said serial shift path of said scan path to change the data to be provided to said RAM by alternating to all ~~zero~~ zeroes or all ~~one-by-one-time~~ ones each shift operation clock cycle;

a third selector for feeding an output of said serial shift path of said scan path back to an input of said serial shift path; and

a gate circuit for detecting that data output from said RAM via said inverters take a specified value.

13. (Currently Amended) The semiconductor integrated circuit according to claim 10, wherein said functional block consists of a RAM, and said semiconductor integrated circuit further comprises:

a plurality of inverters interposed into said serial shift path of said scan path to change the data to be provided to said RAM by alternating to all ~~zero~~ zeroes or all ~~one-by-one-time~~ ones each shift operation clock cycle;

a third selector for feeding an output of said serial shift path of said scan path back to an input of said serial shift path; and

a gate circuit for detecting that data output from said RAM via said first selectors take a specified value.

14. (Currently Amended) The semiconductor integrated circuit according to claim 10, wherein said functional block consists of a RAM, and said semiconductor integrated circuit further comprises:

a plurality of inverters interposed into said serial shift path of said scan path to change the data to be provided to said RAM by alternating to all ~~zero~~ zeroes or all ~~one-by-one-time~~ ones each shift operation clock cycle;

a third selector for feeding an output of said serial shift path of said scan path back to an input of said serial shift path; and

a gate circuit for detecting that data output from said RAM and stored in said flip-flops take a specified value.

15. (Original) The semiconductor integrated circuit according to claim 1, wherein said functional block consists of a RAM, and said first selectors and said second selectors consist of AND-OR compound gate type selectors.

16. (Original) The semiconductor integrated circuit according to claim 1, wherein said functional block consists of a RAM, and said first selectors and said second selectors consist of AND-OR compound gate type selectors and AND-NOR compound gate type selectors.

17. (Currently Amended) The semiconductor integrated circuit according to claim 1, wherein said functional block consists of a RAM, and said semiconductor integrated circuit further comprises:

a plurality of inverters interposed into said serial shift path of said scan path to change the data to be provided to said RAM by alternating to all ~~zero~~ zeroes or all ~~one-by-one-time~~ ones each shift operation clock cycle;

a third selector for feeding an output of said serial shift path of said scan path back to an input of said serial shift path;

a gate circuit for detecting that odd-numbered bit data output from said RAM via said scan path take a specified value; and

a gate circuit for detecting that even-numbered bit data output from said RAM via said scan path take a specified value.

18. (Currently Amended) The semiconductor integrated circuit according to claim 1, wherein said functional block consists of a RAM, and said semiconductor integrated circuit further comprises:

a plurality of inverters interposed into said serial shift path of said scan path to change the data to be provided to said RAM by alternating to all ~~zero~~ zeroes or all ~~one-by-one-time~~ ones each shift operation clock cycle;

a third selector for feeding an output of said serial shift path of said scan path back to an input of said serial shift path;

a gate circuit for detecting that data output from said RAM via said scan path take a specified value; and

a fail flag generator for producing a fail flag signal to cancel a next RAM test and carry out fault analysis, when said gate circuit detects that the data from said RAM differ from the specified value, and for switching said second selectors to said serial shift path.